EK-BM873-TM-004

BM873 1000.08
restart/loader

digital equipment corporation · maynard. massachusetts

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CHAPTER 1
DESCRIPTION

1.1 INTRODUCTION

This manual describes the operation and theory of the BM873 Restart/Loader. This option is intended for use with the PDP-11 family of processors. The BM873

- serves as general purpose loader for processors of the 11 family,
- contains bootstrap loaders for all common devices,
- provides the capability of loading with a "hidden console",
- permits starting from several sources e.g., pushbutton, Watchdog Timer, MODEM control, power fail, etc.,
- gives PDP-11 systems an initial program load capability,
- contains at least four starting addresses, and
- permits the calling of a special user ROM program.

It is assumed that the reader is thoroughly familiar with the operation of the PDP-11 processor with which this option is used.

1.2 GENERAL DESCRIPTION

The BM873 option is contained on a quad-height, extended length module that plugs into a small peripheral controller (SPC) slot. There are four versions of the BM873: YA, YB, YC, and YD. They are described in Table 1-1.

The programs contained in the BM873 can be loaded either from the processor console (Load Address and Start), by a JMP instruction in the program, or by an external contact closure or voltage level. An 8-pin Mate-N-Lok connector is used for the external interface. BM873 specifications are listed in Table 1-2.

1.3 FUNCTIONAL DESCRIPTION

The BM873 consists of two basic sections: the Restart Sequencer and the ROM.

Figure 1-1 shows the remote start timing. The Restart Sequencer takes contact closures or voltage levels and, after filtering and delaying, sets one of four Start Address Select flip-flops. The setting of one of the flip-flops causes the Begin Load Sequence flip-flop to set; this, in turn, initiates two one-shots to create a BUS AC LO/BUS DC LO

Table 1-1
Description of BM873 Versions

Version Designation	ROM Size	Description
BM873-YA	128 words (256 words optional)	Contains bootstrap loader programs for several peripheral devices (RF11, RK11, TC11, etc.).
BM873-YB	256 words	Contains bootstrap loader programs for the devices contained in the YA version, plus programs for the Massbus devices.
BM873-YC	256 words	Contains bootstrap loader programs for the devices contained in the YA version, plus the program for the DU11 Synchronous Interface.
BM873-YD	256 words	Contains bootstrap loader programs for the TC11 DECtape, RH11/RP04 Disk, and the DTE20 10/11 Interface.

Table 1-2
BM873 Specifications

Capacity	
BM873-YA	128 words, read only (256 words optional)
BM873-YB, YC, YD	256 words, read only
Word length	16 bits
ROM cycle time	500 ns
Voltage requirements	+5 V ±5% −15 V ±5%
Current requirements	1.0 A max @ +5 V 2.0 mA max @ −15 V
Operating temperature	10° to 50° C
Humidity	20% to 95%

sequence. The processor responds to the sequence by performing its normal power-down and power-up trap routines. Prior to the power-up sequence, however, the BM873 option asserts 773000 on the Unibus Address Lines. As a result, when the Program Counter (PC) and Processor Status Word (PSW) are restored, the data is taken from locations 773024/26 (nonvolatile memory systems) or from locations 773224/26 (volatile memory systems). Both of these addresses are locations within the BM873 option. The data from 773*24 is 173000; the data from 773*26 is 340, establishing a priority level of 7.

The data read from 773*24 (173000) will have an offset address ORed onto Offset Address bits 8 through 1, giving a range of 173000 to 173776. The offset address bits are enabled by one of the four Start Address Select flip-flops via a diode matrix (Paragraph 2.1.1). Each bootstrap loader program has its own starting address, and it is this address that is selected via the offset address bits.

In the BM873-YB, some of the bootstrap loader programs have two starting addresses. The first address automatically selects unit zero and the second address selects the unit specified in the switch register. See Appendix A for device starting addresses for all versions.

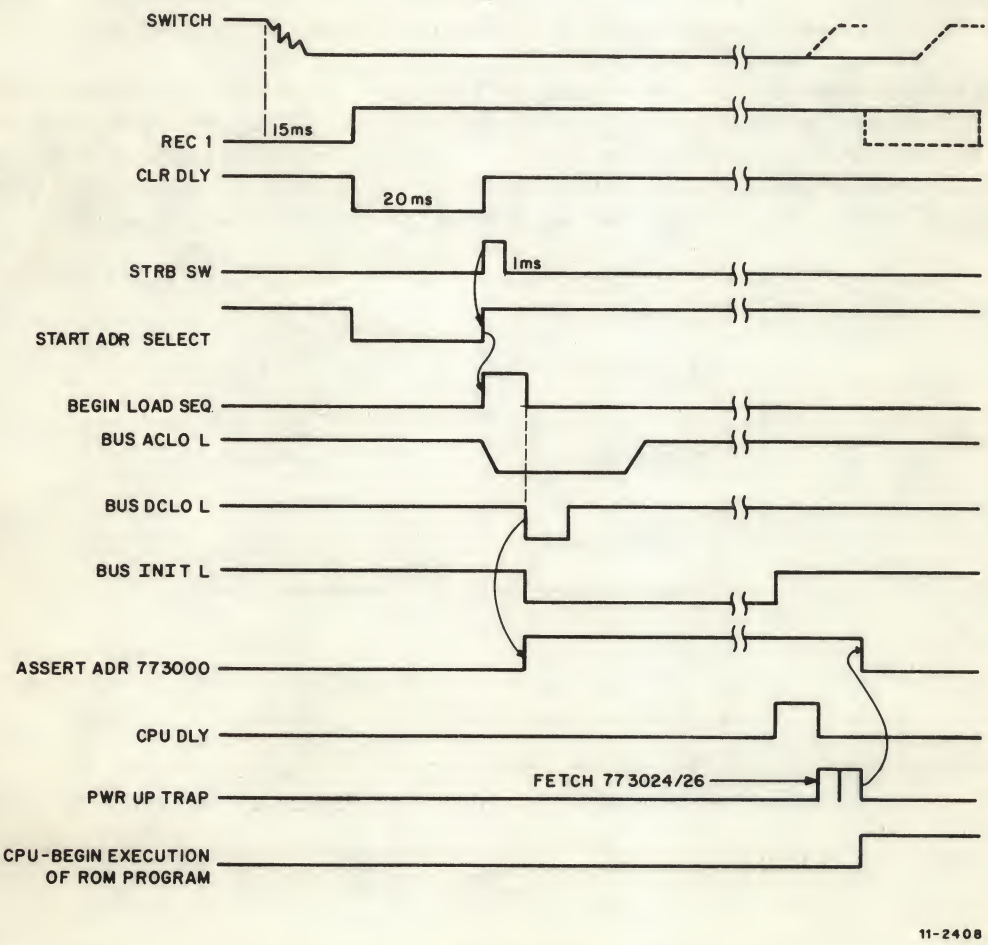


Figure 1-1 Remote Start Timing

The following sequence of operations would be typical:

- Close external switch and wait for switch filter delay.
- Assert AC LO; wait 6 ms.
- Assert DC LO for 6 ms; then wait 8 ms.
- Drop AC LO and assert address 773000.
- Wait for INIT to finish.
- The processor enters power-up routine.
- The BM873 option recognizes the fetch of address 773024 or 773224 and asserts 173XXX plus the 8-bit offset address to the data lines.
- The processor reads location 773026 or 773226 which is always 000340 (priority level 7).
- The processor fetches the next instruction from the ROM in address range 773000–773776. From this point, the bootstrap loader program contained in the ROM has control. (In the PDP-11/35 and PDP-11/40 systems, the PSW is fetched before the PC.)

If an actual power fail occurs in a nonvolatile memory system, the BM873 option does nothing, and the power-down and power-up traps work in the normal manner. If an actual power fail occurs in a volatile memory system, the power-up jumpers in the processor are set for 173224. During power-up the processor will fetch from 173224; the combination of address 773224 and no external lines asserted will cause the BM873 option to assert line 1 as a default case. Thus, in this case, the offset address selected for line 1 becomes the bootstrap loader call for power fail.

Data is read from the ROM in two bytes. Address bits 7 through 1 are present at all times via the bus receivers. Address bit 0 is generated on the module. A0 is always clear prior to a read cycle. The setting of A0 clocks the first byte into a holding register and simultaneously changes the address to gate the second byte to the output drivers. After a delay of about 200 ns, the output gates are enabled and the ROM data is placed on the Unibus. SSYN is asserted about 150 ns later, completing the read cycle. Figure 1-2 illustrates memory read timing.

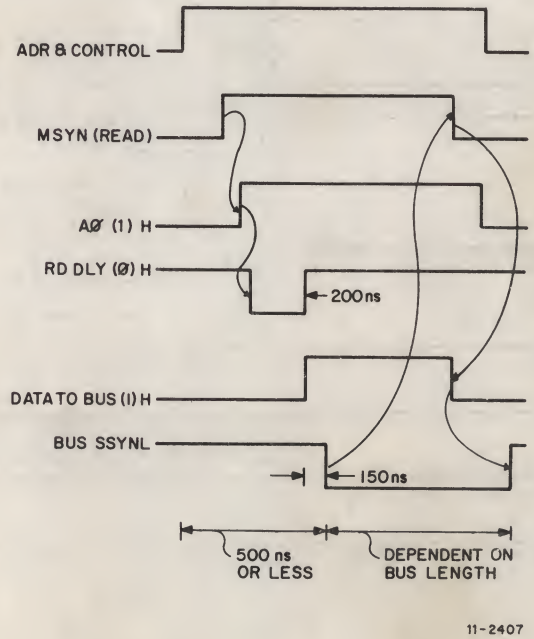


Figure 1-2 Memory Read Timing

CHAPTER 2
INSTALLATION AND CHECKOUT

2.1 INSTALLATION

Normally the BM873 Restart/Loader is installed at the factory and no further installation is required. However, if this option is added to an existing system, it may be necessary to add wiring to make the AC LO and DC LO signals available. These signals are provided on the PDP-11/05 and PDP-11/45 processors, and on the DD11-B. On the PDP-11/15, PDP-11/20, PDP-11/35, PDP-11/40, and the DD11-A it is necessary to ensure that the SPC slot containing the BM873 has BUS AC LO and BUS DC LO wiring available as follows:

Pin CV1 to B01F1 or B04F1 (BUS AC LO)

Pin CN1 to B01F2 or B04F2 (BUS DC LO)

If the wiring is not present, it must be added by hand-wiring, using a wire color different from that of the existing backplane wiring.

NOTE
The BM873 option must be on the CPU side of any bus buffer.

2.1.1 Start Address Selection

Each of the four external interface circuits has an associated address which must be specified for that circuit to be addressed. Each address consists of a fixed high-order portion (773XXX) and a low-order portion (bits 8 through 1) that is selected by adding or cutting diodes (Figure 2-1). With the diode in, a 1 is placed on the Unibus. With the diode out, a 0 is placed on the Unibus. When adding diodes, a low-wattage iron should be used and care should be taken with the plated mounting holes, so that the plating is not lifted from the laminate by the heat. The diodes (DEC type 664 or 1N3606) should be positioned so that their cathodes point toward the gold fingers of the module.

Appendix A lists starting addresses for various devices used with the BM873-YA, -YB, -YC and -YD Restart/Loaders. The three rightmost digits of the address represent the low-order portion to be selected via diodes.

The diagnostic program for this option contains a listing of the loader program in the comments portion of the Data Compare section. That diagnostic will be updated to contain the starting addresses and listing of future variations.

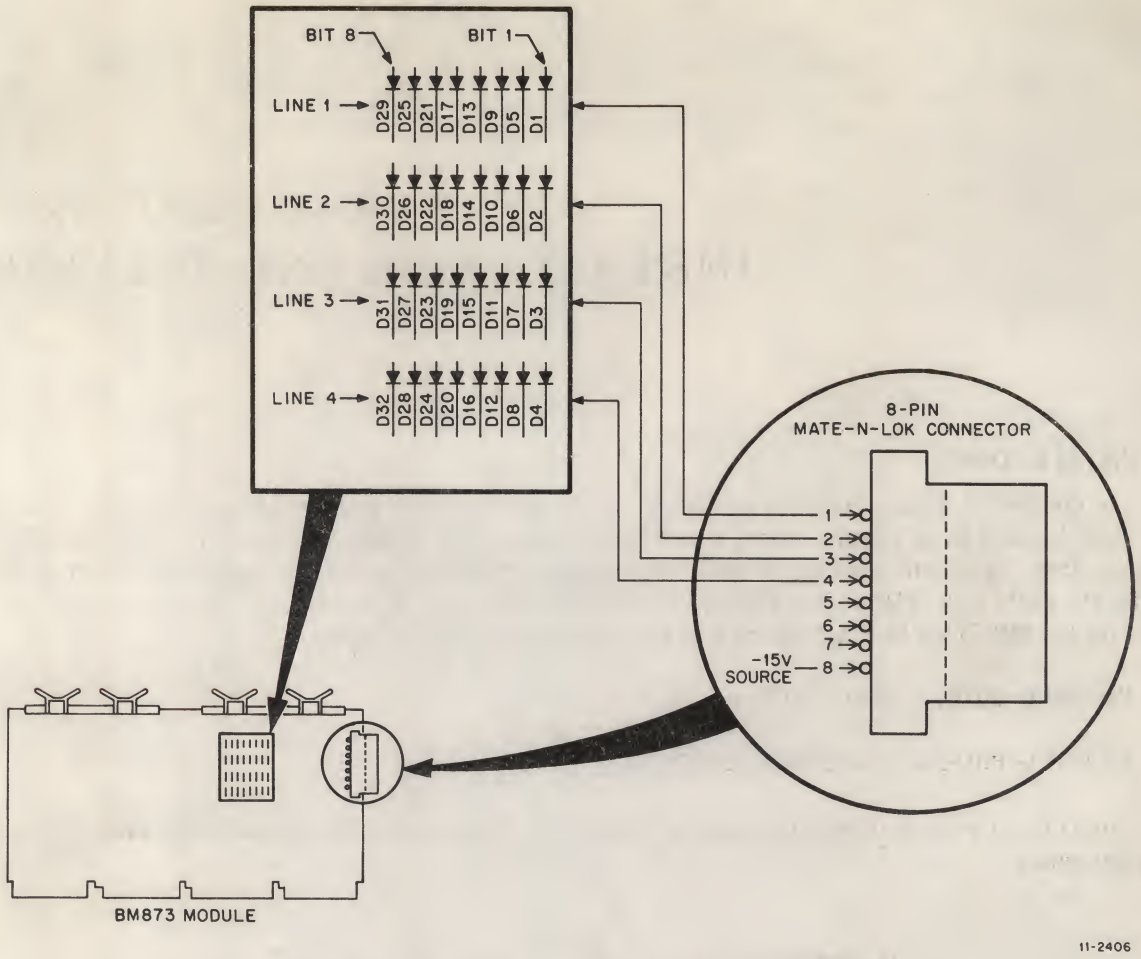


Figure 2-1 External Interface Circuit Diode Matrix

2.1.2 Jumper Selection

The BM873 module contains three jumpers that are marked with the numerals 1, 2, and 3. Jumpers 1 and 2 are used to compensate for differences between the PDP-11/40 and 11/35 and all other PDP-11 family processors. Jumper 1 should be installed when the option is used with either the PDP-11/40 or the PDP-11/35. Jumper 2 should be installed for use with any other processor in the PDP-11 family. For the BM873-YD, jumper 1 is always installed and jumper 2 is always removed. Resistor R3 is also removed on the BM873-YD.

Jumper 3 controls access to an extra 128 words of ROM. When this jumper is cut, additional addresses from 773400 to 773776 become available. For the BM873-YB, -YC, and -YD versions, this jumper is always cut.

2.1.3 CPU Addressing with Volatile Memory

When this option is used in computers with volatile memory, the power fail trap address must be jumpered to 773224 if automatic reloading is desired.

For a PDP-11/45 CPU, install jumpers W6, W3, and W1 on the M8100 board. This will provide an address of 773224.

For a PDP-11/40 CPU, connect jumper W7 on the M7235 board for a binary 1. This jumper will provide an address of 7732XX. The last two digits are provided by jumpers 4 and 2.

2.2 CHECKOUT

The diagnostic program for the BM873 option is MAINDEC-11-DZBMD-D. This program starts with a dialogue and is self-explanatory. As new ROM programs are implemented, this diagnostic may be modified. However, the basic version may be used on all option variations as long as the user visually checks the ROM data following the first pass.

The diagnostic contains the instructions for its own operation. The opening dialogue establishes which option variation (-YA, -YB, etc.) is being tested.

CHAPTER 3
PROGRAMMING

This device is a Read-Only Memory and requires no programming. However, certain factors must be considered in system programming as the following paragraphs explain.

3.1 POWER FAIL PROGRAMMING

With the BM873 option installed, the power-down/power-up routines may require modification, depending on the bootstrap used. Use of the external interface causes the power-fail sequence in the CPU when AC LO is detected going low; the power-up trap program is not used, and, therefore, not restored.

This is not a problem when a bootstrap loads into core and overwrites location 24, because the new program will set up the power-fail routine. However, if the new program does not reload location 24, the next power-fail sequence (may be real) will find the power-up restore program instead of the power-down routine.

This condition can be resolved by the power-fail routine testing this option with any DATI instruction. The combination of this option and a real power-fail will cause the DATI to perform in a normal manner. The combination of this option and the external interface active (causing the AC LO and trap) will cause a nonexistent device trap (no SSYN) to location 4.

```
        MOV             #1S,@#4         ; TRAP CATCHER
        CLR             @#6
        TST             @#173000        ; DEV BLIND?
        NOP
2S:     MOV             #PWRUP,@#24     ; REAL PWR FAIL
        (SAVE ROUTINE)
1S:     HALT
```

Example 1

The above program works because this option goes "blind" (will not return SSYN) when it has been activated by an external interface signal. This condition continues from the assertion of AC LO until the release of DC LO.

3.2 REGISTER DESCRIPTION

There are no registers in this device. There are four flip-flops that can be loaded for diagnostic purposes but they cannot be read.

CHAPTER 4
OPTIONS

4.1 USER CUSTOM PROGRAM FOR THE BM873-YA

Two etched circuit positions on the BM873-YA board provide an extra 128 words of ROM. To add this extra memory capacity, Jumper 3 must be cut, permitting address recognition of all 256 words.

Figure 4-1 is a sample ROM program data sheet that can be helpful in programming the ROMs. Columns 1 and 2 contain the PDP-11 program listing. From the address data in column 1, the ROM starting address can be determined and the offset diodes cut (diode = 1; no diode = 0). The data in column 2 must be expressed in binary form as in columns 3 and 4. (Note that byte 1 is moved to the line below that of the original entry.) The eight binary digits for each byte are then shifted into columns 5 and 6 under the ROM B and ROM A headings, respectively. Columns 7 and 8 contain the resulting ROM address in binary and decimal form, respectively. Column 8 consists of four columns of decimal addresses, distinguished by the configuration of the 2 MSB of the binary address. Each program data sheet contains 64 ROM locations (32 words), hence four sheets are required to encode all 128 words. Therefore, only one of the four subcolumns of decimal addresses actually applies for each sheet, and the other three should be crossed out to avoid confusion. The 2-column checklist between columns 7 and 8 can be used for checkoff purposes, e.g., checking off ROMs as they are blasted.

A blank program data sheet is included in Chapter 6 to assist the user in programming the read-only memory of the BM873.

Customers who wish to create their own programs can purchase PROMs from integrated circuit vendors or distributors. Some distributors have programming capabilities so that programmed ROMs can be purchased. The following PROMs have been found acceptable:

Intersil type 5603A
Monolithic Memories Inc. type 6300

The following PROMs have not been tested but according to the manufacturer's data should be acceptable. Any PROM that is specified to be "pin compatible with the 74187" should work in this application.

National Semiconductor type DM8573
Signetics type 82S26

Sheet of 4

Choose one of four sheets. Cross out the other three address lists.

ROM Program Data Sheet – 32_{10} Word Block

Program Listing Addr.	Program Listing Data	Octal List Byte "1"	Octal List Byte "0"	ROM "B" 3 2 1 0	ROM "A" 3 2 1 0	ROM Addr. 5 4 3 2 1	0	A	B	1 ↓ 7 6	2 ↓ 7 6	3 ↓ 7 6	4 ↓ 7 6
										Address Bits 7 & 6			
										00	01	10	11
173000	010702		11 000 010	1100	0010	00000	0	✓	✓	0	64	128	192
		0 001 000 1		0001	0001		1	✓	✓	1	65	129	193
173002	000455		00 101 101	0010	1101	00001	0	✓	✓	2	66	130	194
		0 000 000 1		0000	0001		1	✓	✓	3	67	131	195
173004	177462		00 110 010	0011	0010	00010	0	✓		4	68	132	196
		1 111 111 1		1111	1111		1	✓		5	69	133	197
173006	000005		00 000 101	0000	0101	00011	0	✓		6	70	134	198
		0 000 000 0		0000	0000		1	✓		7	71	135	199
173010	010702		11 000 010	1100	0010	00100	0	✓		8	72	136	200
		0 001 000 1		0001	0001		1	✓		9	73	137	201
173012	000451		00 101 001	0010	1001	00101	0	✓		10	74	138	202
		0 000 000 1		0000	0001		1	✓		11	75	139	203
173014	177406		00 000 110	0000	0110	00110	0	✓		12	76	140	204
		1 111 111 1		1111	1111		1	✓		13	77	141	205
			00		0000	00				14	78		206
173066	000423		00 010 011	0001		11011	0	✓			118	182	246
		0 000 000 1		0000	0001		1	✓		55	119	183	247
173070	176716		11 001 110	1100	1110	11100	0	✓		56	120	184	248
		1 111 110 1		1111	1101		1	✓		57	121	185	249
173072	000005		00 000 101	0000	0101	11101	0	✓		58	122	186	250
		0 000 000 0		0000	0000		1	✓		59	123	187	251
173074	010702		11 000 010	1100	0010	11110	0	✓		60	124	188	252
		0 001 000 1		0001	0001		1	✓		61	125	189	253
173076	000417		00 001 111	0000	1111	11111	0	✓		62	126	190	254
		0 000 000 1		0000	0001		1	✓		63	127	191	255

Figure 4-1 Sample ROM Program Data Sheet

CHAPTER 5
INTERFACE

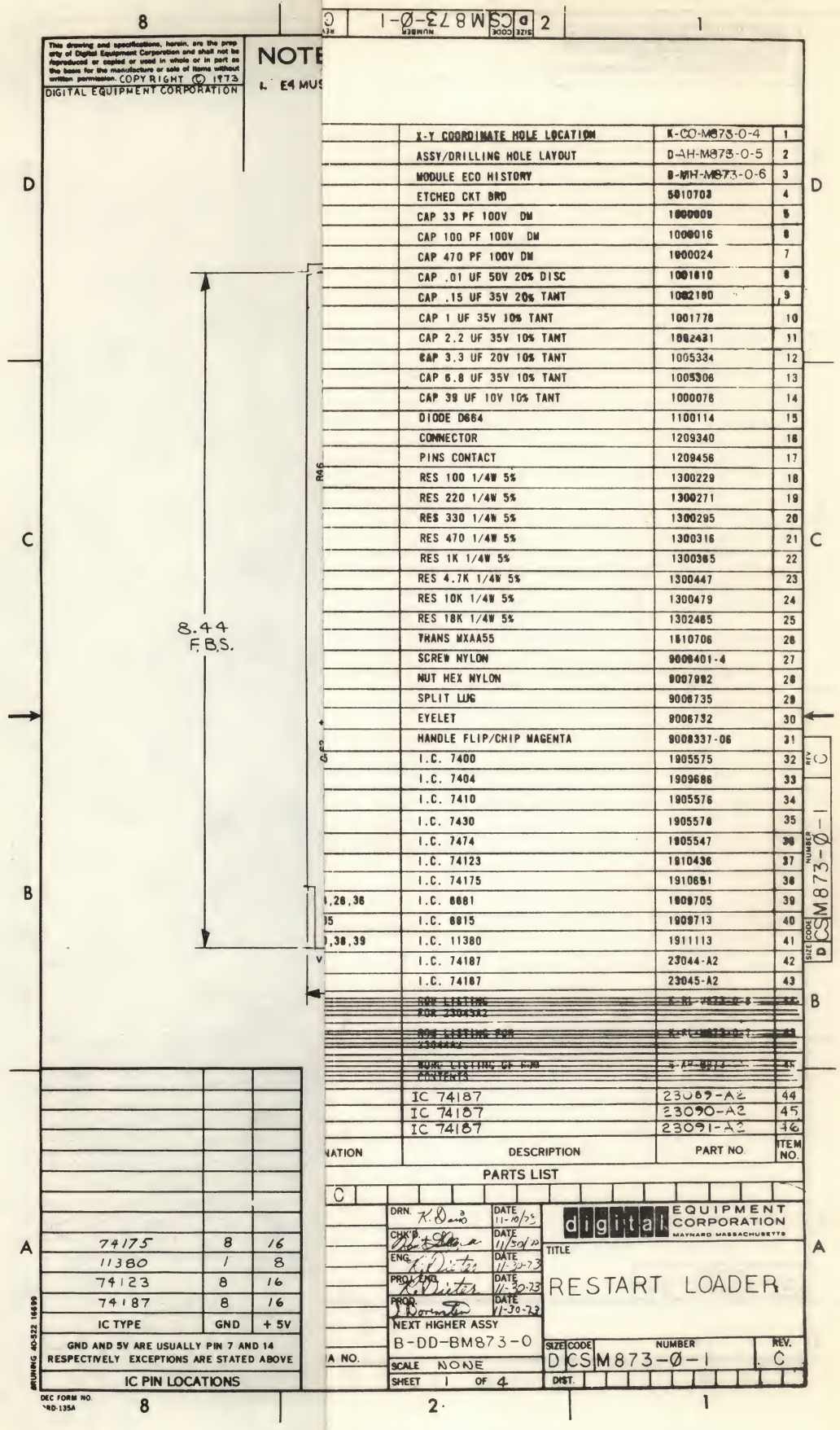
The external interface consists of four separate high-impedance receivers with 4.7-kilohm resistors in series with each one. A -15 V source is provided through 10 kilohms to facilitate the use of contact closures. The external interface also accepts single-ended voltage inputs. A signal of 0.5 mA at -4 V or greater will cause a Restart sequence. The maximum permissible input is ±25 V.

These inputs are filtered with RC networks and Schmitt triggers and have a time delay of approximately 10 to 15 ms. The signal must remain for at least 150 ms. Only one external line may be active at a time; two or more active at the time of the sample will cause a race condition until one wins, but the result will be indeterminate.

The interface connector is an 8-pin male Mate-N-Lok (DEC Part Number 12-09340-01). Five pins (DEC Part Number 12-09378) are required for connection--placed as shown in Figure 2-1.

CHAPTER 6
ENGINEERING DRAWINGS

This chapter contains the 4-sheet engineering drawing of the BM873 (D-CS-M873-0-1) and a blank program data sheet for use in programming the read-only memory of this option. Use of these sheets is described in Chapter 4 of this manual.



ITEM NO.	PART NO.	DESCRIPTION
1	K-CO-M873-0-4	X-Y COORDINATE HOLE LOCATION
2	D-AH-M873-0-5	ASSY/DRILLING HOLE LAYOUT
3	B-MH-M873-0-6	MODULE ECO HISTORY
4	5010703	ETCHED CKT BRD
5	1000009	CAP 33 PF 100V DM
6	1000016	CAP 100 PF 100V DM
7	1000024	CAP 470 PF 100V DM
8	1001810	CAP .01 UF 50V 20% DISC
9	1002190	CAP .15 UF 35V 20% TANT
10	1001778	CAP 1 UF 35V 10% TANT
11	1002431	CAP 2.2 UF 35V 10% TANT
12	1005334	CAP 3.3 UF 20V 10% TANT
13	1005306	CAP 6.8 UF 35V 10% TANT
14	1000078	CAP 39 UF 10V 10% TANT
15	1100114	DIODE D664
16	1209340	CONNECTOR
17	1209456	PINS CONTACT
18	1300229	RES 100 1/4W 5%
19	1300271	RES 220 1/4W 5%
20	1300295	RES 330 1/4W 5%
21	1300316	RES 470 1/4W 5%
22	1300365	RES 1K 1/4W 5%
23	1300447	RES 4.7K 1/4W 5%
24	1300479	RES 10K 1/4W 5%
25	1302465	RES 18K 1/4W 5%
26	1810706	TRANS MXAA55
27	9006401-4	SCREW NYLON
28	9007992	NUT HEX NYLON
29	9006735	SPLIT LUG
30	9006732	EYELET
31	9008337-06	HANDLE FLIP/CHIP MAGENTA
32	1905575	I.C. 7400
33	1909686	I.C. 7404
34	1905576	I.C. 7410
35	1905578	I.C. 7430
36	1905547	I.C. 7474
37	1910436	I.C. 74123
38	1910651	I.C. 74175
39	1909705	I.C. 8881
40	1909713	I.C. 8815
41	1911113	I.C. 11380
42	23044-A2	I.C. 74187
43	23045-A2	I.C. 74187
44	23089-A2	IC 74187
45	23090-A2	IC 74187
46	23091-A2	IC 74187

PARTS LIST

IC TYPE	GND	+ 5V
74175	8	16
11380	1	8
74123	8	16
74187	8	16

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DRN. K. Dano — DATE 11-10-73
CHK'D — DATE 11/30/73
ENG. K. Dieter — DATE 11-30-73
PROJ. ENG. K. Dieter — DATE 11-30-73
PROD. J. Donnelly — DATE 11-30-73
NEXT HIGHER ASSY B-DD-BM873-0
SCALE NONE
SHEET 1 OF 4

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE RESTART LOADER

SIZE D | CODE CS | NUMBER M873-0-1 | REV. C

DIST.

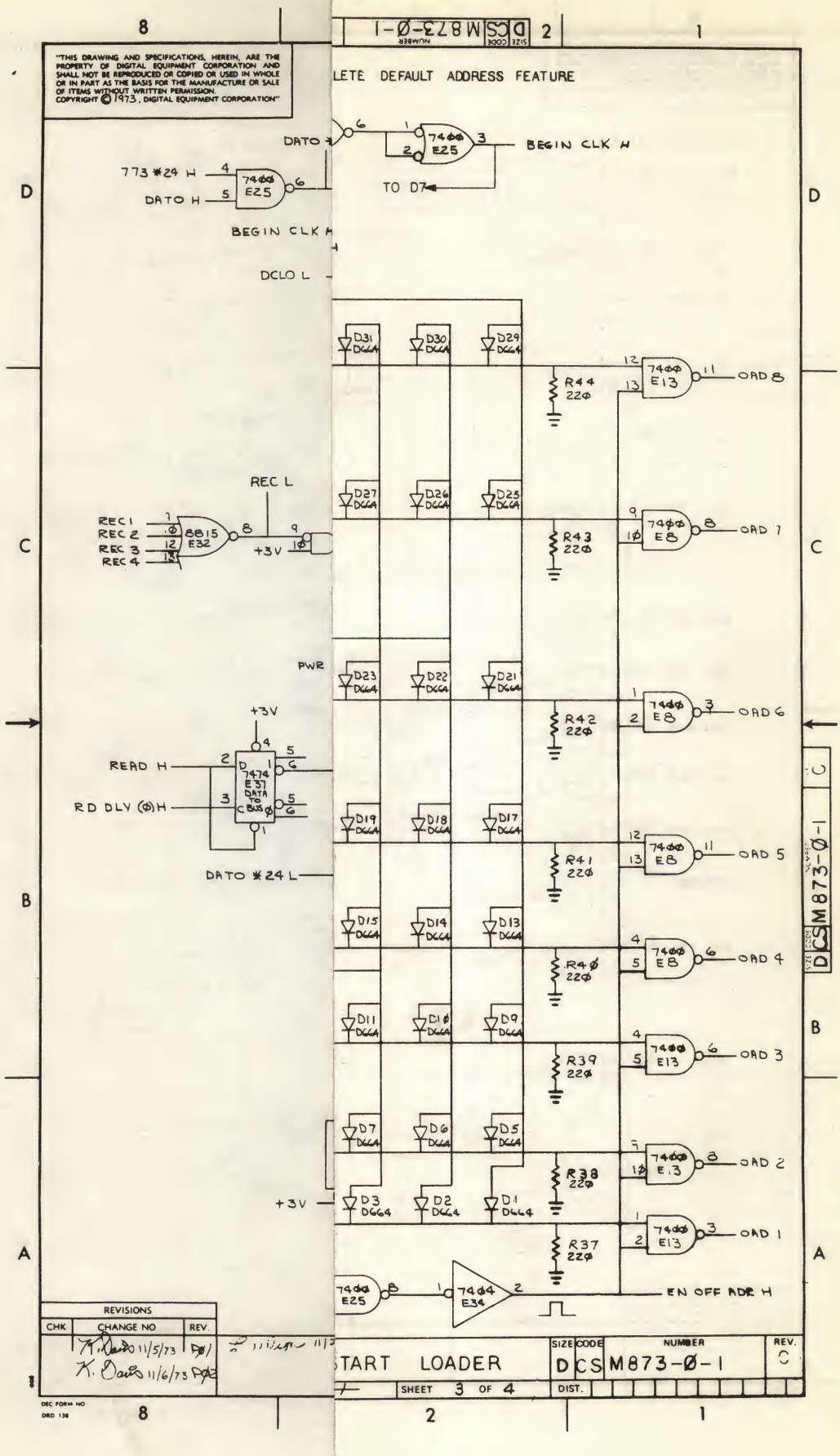
DEC FORM NO. 40-1354

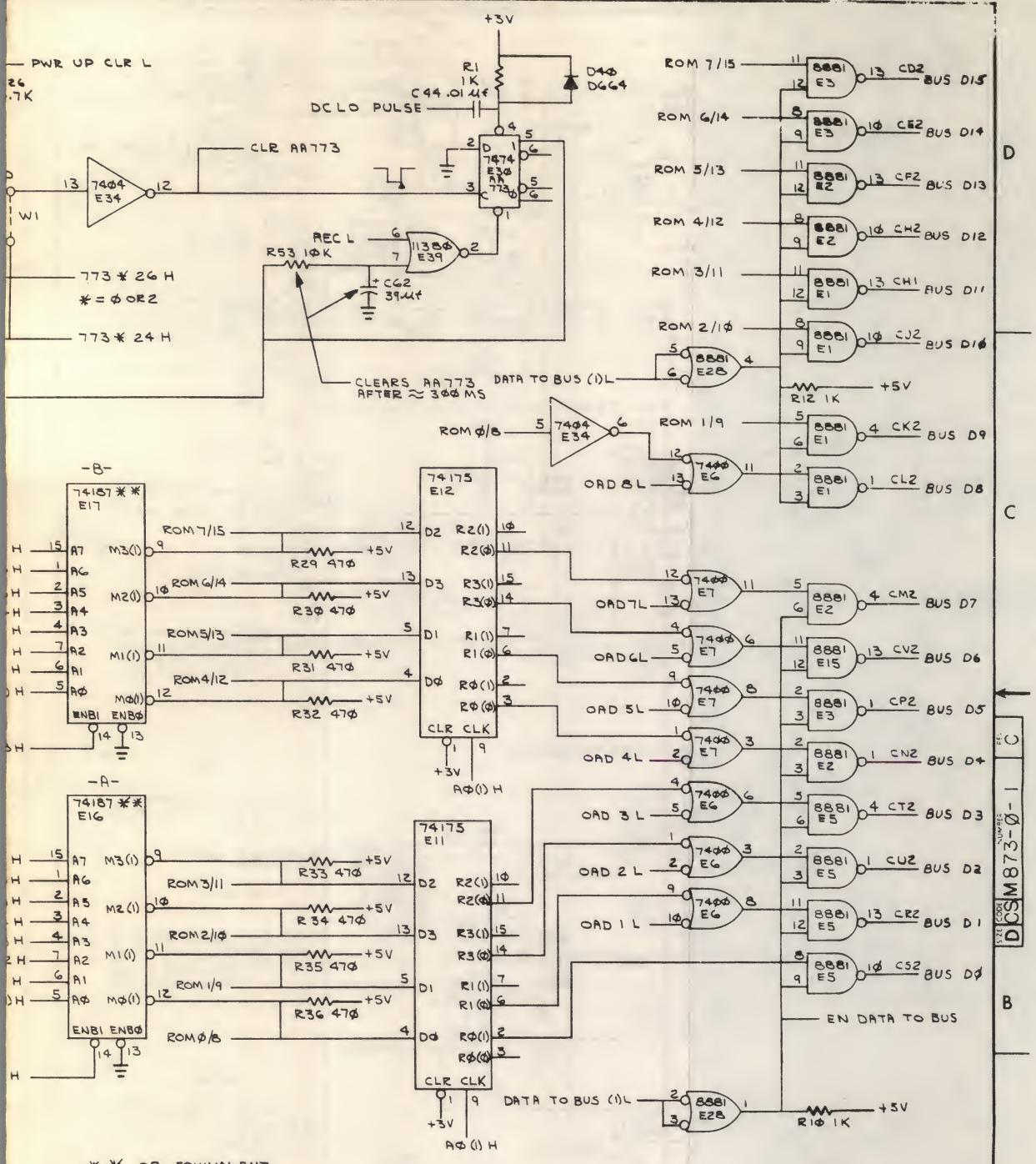
M873-YB	M873-YA	M873-0	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
QTY	QTY	QTY				
A/R	A/R	–	W1,W2,W3	JUMPER	9107560-1	48
1	–	–	E20	IC 74187	23092-A2	47
–	REF	–		ROM LISTING FOR 23045A2	K-RL-M873-0-8	50
–	REF	–		ROM LISTING FOR 23044A2	K-RL-M873-0-7	49
REF	–	–		ROM LISTING FOR 23090 A2	K-RL-M873-0-11	52
REF	–	–		ROM LISTING FOR 23089 A2	K-RL-M873-0-10	51
REF	–	–		ROM LISTING FOR 23091 A2	K-RL-M873-0-12	53
REF	–	–		ROM LISTING FOR 23092 A2	K-RL-M873-0-13	54
–	REF	–		WORD LISTING OF YA ROM CONTENTS	B-AP-M873-0-9	55
REF	–	–		WORD LISTING OF YB ROM CONTENTS	B-AP-M873-0-14	56

PARTS LIST

TITLE	SIZE	CODE	NUMBER	REV.
RESTART LOADER	D	CS	M873-Ø-1	C
SCALE ——	SHEET 2 OF 4	DIST.		

M873-Ø-1 C


"THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT © 1973, DIGITAL EQUIPMENT CORPORATION"
DCS M873-Ø-1
LETE DEFAULT ADDRESS FEATURE
DATO *
7400 E25
BEGIN CLK H
TO D7
773 *24 H
DATO H
7400 E25
BEGIN CLK H
DCLO L
REC L
REC 1
REC 2
REC 3
REC 4
8815 E32
+3V
PWR
+3V
READ H
RD DLY (Φ) H
7474 E37 DATA TO C BUS Φ
DATO *24 L
+3V
D31 D30 D29 DGGA
R44 22Φ
7400 E13
OAD 8
D27 D26 D25 DGGA
R43 22Φ
7400 E8
OAD 7
D23 D22 D21 DGGA
R42 22Φ
7400 E8
OAD 6
D19 D18 D17 DGGA
R41 22Φ
7400 E8
OAD 5
D15 D14 D13 DGGA
R40 22Φ
7400 E8
OAD 4
D11 D10 D9 DGGA
R39 22Φ
7400 E13
OAD 3
D7 D6 D5 DGGA
R38 22Φ
7400 E13
OAD 2
D3 D2 D1 DGGA
R37 22Φ
7400 E13
OAD 1
7400 E25
7404 E34
EN OFF ADR H
REVISIONS
CHK
CHANGE NO
REV.
K. Davis 11/5/73 D01
K. Davis 11/6/73 D02
START LOADER
SIZE C
CODE DCS
NUMBER M873-Ø-1
REV. C
SHEET 3 OF 4
DIST.
DEC FORM NO DRD 138



GRANT JUMPERS

DK2 DL2 DM2 DN2 — DP2 DR2 DS2 DT2

M873-YA	E19, E2Ø	MMI 6300	OPTIONAL
M873-YB	E19, E2Ø	74187 OR EQUIV.	REQUIRED

SEE PARTS LIST

TITLE	SIZE	CODE	NUMBER	REV.
RESTART/LOADER	D	CS	M873-Ø-1	C
SCALE —	SHEET 4 OF 4	DIST.		

ROM Program Data Sheet – 32_{10} Word Block

Sheet of 4

									1 ↓	2 ↓	3 ↓	4 ↓
					1 1 0 0 0	0			48	112	176	240
						1			49	113	177	241
					1 1 0 0 1	0			50	114	178	242
						1			51	115	179	243
					1 1 0 1 0	0			52	116	180	244
						1			53	117	181	245
					1 1 0 1 1	0			54	118	182	246
						1			55	119	183	247
					1 1 1 0 0	0			56	120	184	248
						1			57	121	185	249
					1 1 1 0 1	0			58	122	186	250
						1			59	123	187	251
					1 1 1 1 0	0			60	124	188	252
						1			61	125	189	253
					1 1 1 1 1	0			62	126	190	254
						1			63	127	191	255

Choose one of four sheets. Cross

APPENDIX A
DEVICE STARTING ADDRESSES

BM873-YA Starting Addresses

Address	Device Type
773000	RF11 DECdisk
773010	RK11 Disk
773020	Transfer to address contained in switch register
773030	TC11 DECtape
773050	TM11 DECmagtape
773100	RP11 Disk Pack
773144	RC11 Disk
773210	KL11/DC11 Console TTY Reader
773230	TA11 Cassette
773312	PC11 Paper Tape Reader

BM873-YB Starting Addresses

Address	Device Type
773000	RH11/RS03/RS04 Disk (Unit zero)
773002	RH11/RS03/RS04 Disk (Unit specified in switch register)
773030	RK11 Disk (Unit zero)
773032	RK11 Disk (Unit specified in switch register)
773070	TC11 DECtape
773110	TM11 DECmagtape
773136	RF11 DECdisk
773150	RH11/TU16/TM02 Tape Drive
773212	RC11 Disk
773230	RH11 Device Combination (Unit zero)*
773231	RH11 Device Combination (Unit specified in switch register)
773320	RH11/RP04 Disk (Unit zero)
773322	RH11/RP04 Disk (Unit specified in switch register)
773344	Transfer to address contained in switch register
773350	RP11 Disk Pack (Unit zero)
773352	RP11 Disk Pack (Unit specified in switch register)
773510	KL11/DL11 Console TTY Reader
773524	TA11 Cassette (Unit zero)
773526	TA11 Cassette (Unit specified in switch register)
773620	PC11 Paper Tape Reader

*If the TM02/TU16 is selected, the value in the console switch register is the position of the TM02 on the RH11, instead of the unit number on the TU16 drive. The slave unit number (number on TU16) should still be zero.

BM873-YC Starting Addresses

Address	Device Type
773000	RF11 DECdisk
773010	RK11 Disk
773020	Transfer to address contained in switch register
773030	TC11 DECtape
773050	TM11 DECmagtape
773100	RP11 Disk Pack
773144	RC11 Disk
773210	KL11/DC11 Console TTY Reader
773230	TA11 Cassette
773312	PC11 Paper Tape Reader
773400	DU11 Synchronous Interface

BM873-YD Starting Addresses

Address	Device Type
773000	Transfer to address contained in switch register
773014	TC11 DECtape
773304	RH11/RP04 Disk
773534	DTE20 10/11 Interface

Reader's Comments

BM873 RESTART/LOADER
EK-BM873-TM-004

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

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